Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.091”**

**.139”**

**GATE**

**SOURCE**

**Top Material: Al**

**Backside Material: AlTiNi**

**Bond Pad Size: .015” X .030”**

**Backside Potential: DRAIN**

**Mask Ref: GEN V**

**APPROVED BY: DK DIE SIZE .091” X .139” ATE: 11/9/21**

**MFG: RCA THICKNESS .005” P/N: IRFC521**

**DG 10.1.2**

#### Rev B, 7/19/02